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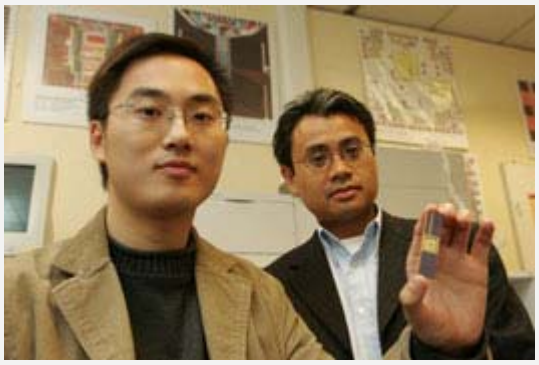
Innovative Design Technologies Presented at Chip Olympics

Two researchers from the Hong Kong University of Science and Technology (HKUST) present their innovative integrated circuits design technology today (8 February 2005) at the International Solid-State Circuits Conference, also known as the "Chip Olympics". Their novel designs will help manufacturers create portable electronics more compact in size, and wireless equipment capable of carrying more data for future multimedia applications.

This year's "Chip Olympics" are being held from 6 to 10 February in San Francisco. HKUST researchers have been invited to present their research findings at the Conference almost every year since 1997. To date, HKUST is the only university from Hong Kong to appear at this international event.

Dr Hoi Lee, a 2004 PhD graduate of the University's Electrical and Electronic Engineering Department (ELEC), is successfully finding improved ways to design power management integrated circuits for new generation portable electronics, whose demands for lower supply voltage and longer battery lifespan are increasingly high.



Dr Hoi Lee (left) and his supervisor Dr Philip Mok present their innovative power management integrated circuits

By implementing switched-capacitor power converter modules and the novel pseudo-continuous output regulation technology that alternately regulate the output voltage without hampering performance, Dr Lee has reduced the chip size of power management integrated circuits by 20% and the capacitor values by 10 times, in turn reducing production costs by five times.

Wing Lun Ng, MPhil student of ELEC, is addressing the performance issue of high frequency wireless applications in which voltage and power consumption increase as transmission frequency rises.

The PLL chip developed by Wing Lun Ng (right) and his supervisor Dr Howard Luong can output signals as high as 24 GHz

Ng and his team developed novel ultra-low-voltage high frequency components in a phase locked loop (PLL), the crucial device in wireless applications, and to "recycle" their electric current, thereby minimizing total power consumption. He has created a prototype fabricated with the cheapest complementary metal oxide semiconductor (CMOS) process that has achieved a 24 GHz output frequency which is among the fastest in the world with the lowest supply voltage of 1V and very low power consumption.

Dr Hoi Lee and Ng expressed their gratitude to their supervisors Dr Philip Mok and Dr Howard Luong for their dedicated guidance. In addition, they commended the University for building up its strengths in IC design for power management and for wireless

communication, facilitating an environment for brainstorming and new ideas.

From Left: Dr Philip Mok, Dr Hoi Lee, Wing Lun Ng and Dr Howard Luong at the Chip Olympics in San Francisco